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(54) **CONNECTING TECHNIQUES FOR STACKED CMOS DEVICES**

(71) Applicant: **Taiwan Semiconductor Manufacturing Co., Ltd.**, Hsin-Chu (TW)

(72) Inventors: **Hsiang-Jen Tseng**, Hsinchu (TW); **Wei-Yu Chen**, Hsinchu (TW); **Ting-Wei Chiang**, New Taipei (TW); **Li-Chun Tien**, Tainan (TW)

(73) Assignee: **Taiwan Semiconductor Manufacturing Co., Ltd.**, Hsin-Chu (TW)

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H01L 23/48	(2006.01)
H01L 21/822	(2006.01)
H01L 27/06	(2006.01)
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H01L 21/74	(2006.01)
H01L 23/522	(2006.01)
H01L 23/532	(2006.01)

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CPC ***H01L 21/76838*** (2013.01); ***H01L 21/743*** (2013.01); ***H01L 21/8221*** (2013.01); ***H01L 23/481*** (2013.01); ***H01L 23/528*** (2013.01); ***H01L 23/535*** (2013.01); ***H01L 24/29*** (2013.01); ***H01L 24/32*** (2013.01); ***H01L 24/48*** (2013.01); ***H01L 24/73*** (2013.01); ***H01L 24/83*** (2013.01); ***H01L 25/0652*** (2013.01); ***H01L 25/0657*** (2013.01); ***H01L 25/50*** (2013.01); ***H01L 27/0688*** (2013.01); *H01L 23/522* (2013.01); *H01L 23/53223* (2013.01); *H01L 23/53238* (2013.01); *H01L 23/53252* (2013.01); *H01L 23/53266* (2013.01); *H01L 2225/06527* (2013.01); *H01L 2225/06548* (2013.01); *H01L 2924/13091* (2013.01)

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CPC ... H01L 25/0657; H01L 24/48; H01L 24/73; H01L 24/29; H01L 24/32; H01L 23/481; H01L 24/83

See application file for complete search history.

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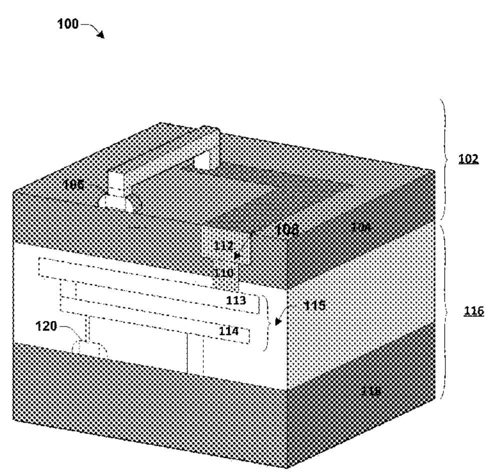
Primary Examiner — Ngan Ngo

(74) *Attorney, Agent, or Firm* — Eschweiler & Associates, LLC

(57) **ABSTRACT**

A stacked integrated circuit includes multiple tiers vertically connecting together. A multi-layer horizontal connecting structure is fabricated inside a substrate of a tier. Layers of the horizontal connecting structure have different patterns as viewed from above the substrate.

19 Claims, 7 Drawing Sheets



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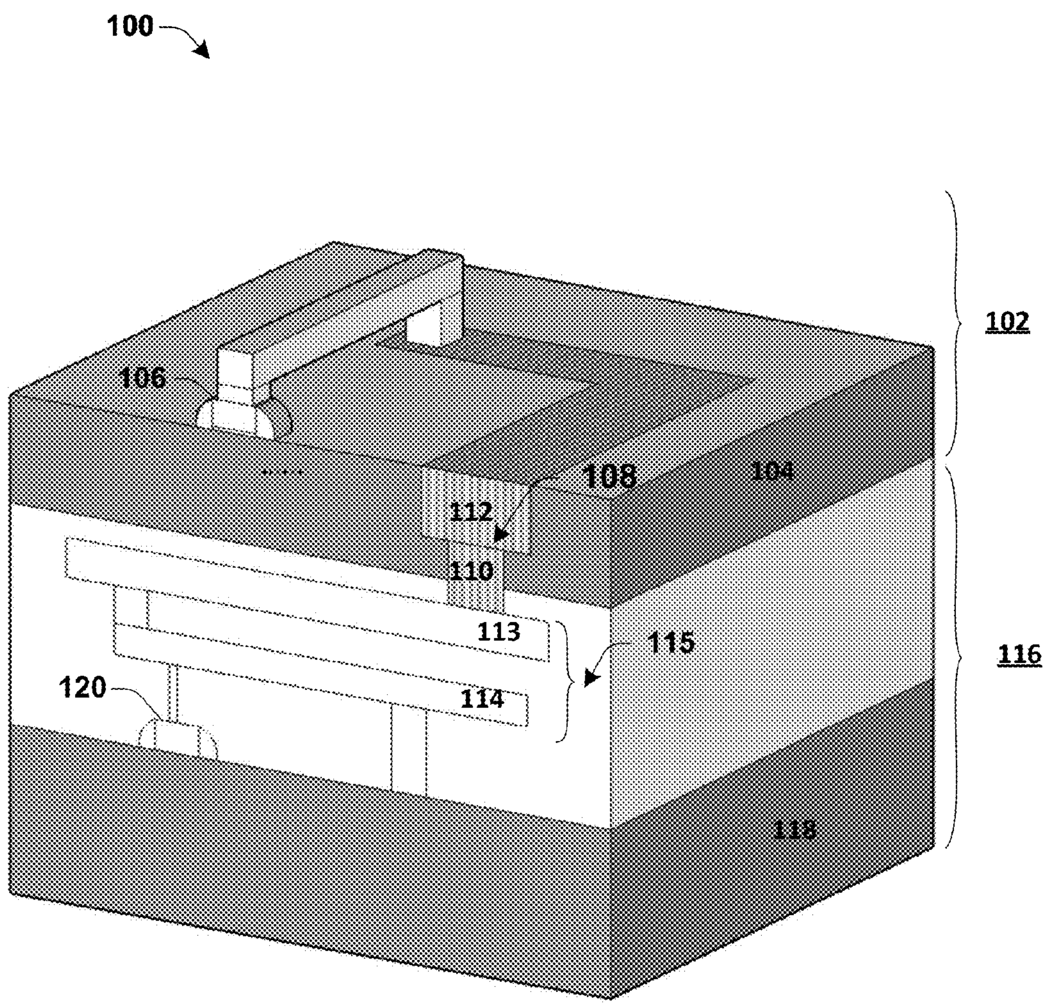
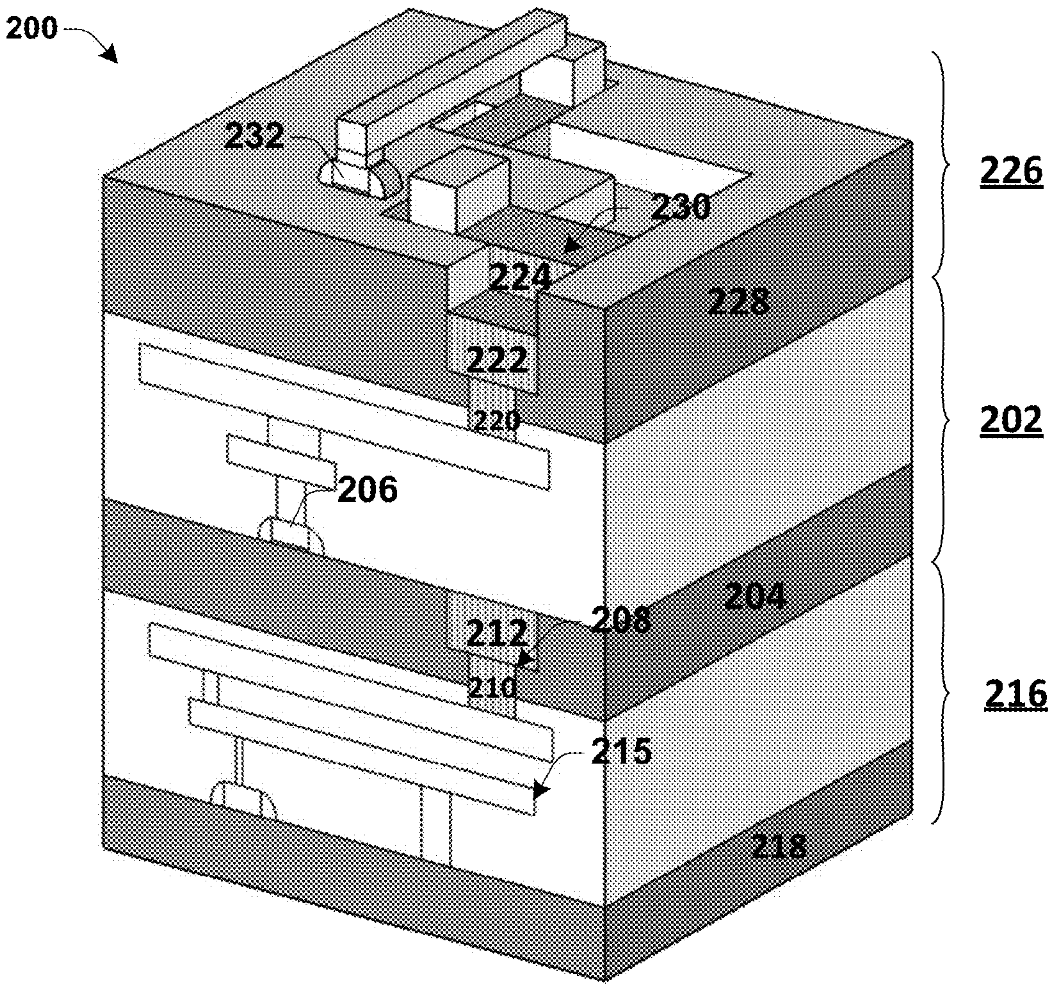


FIG. 1


200
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218

FIG. 2

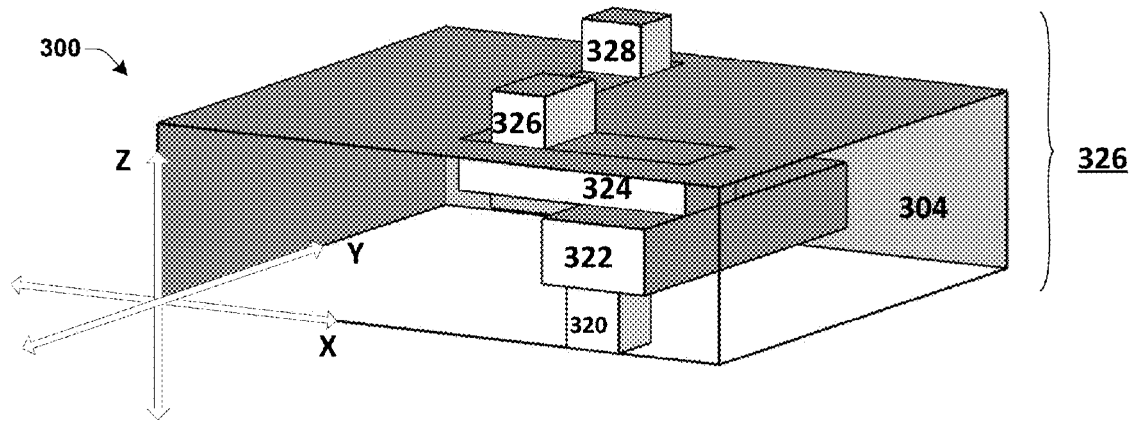


FIG. 3

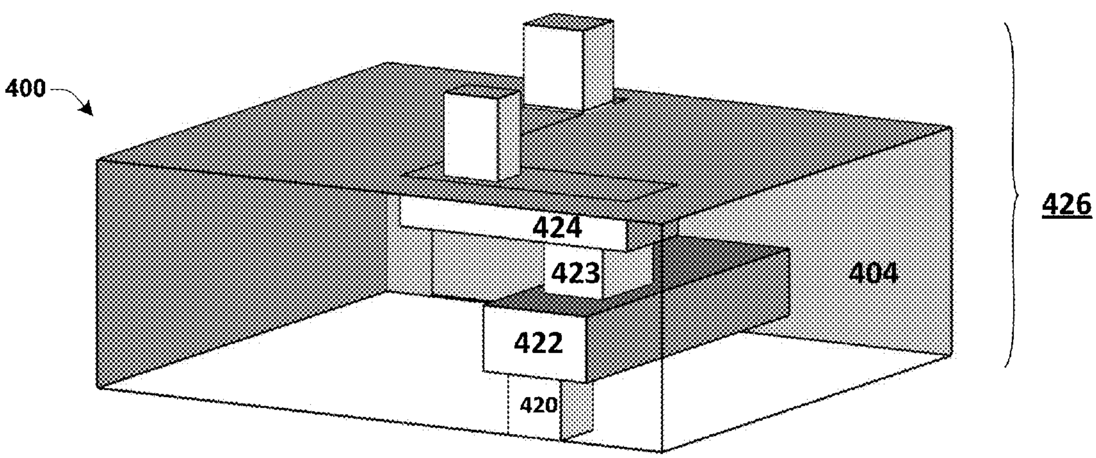
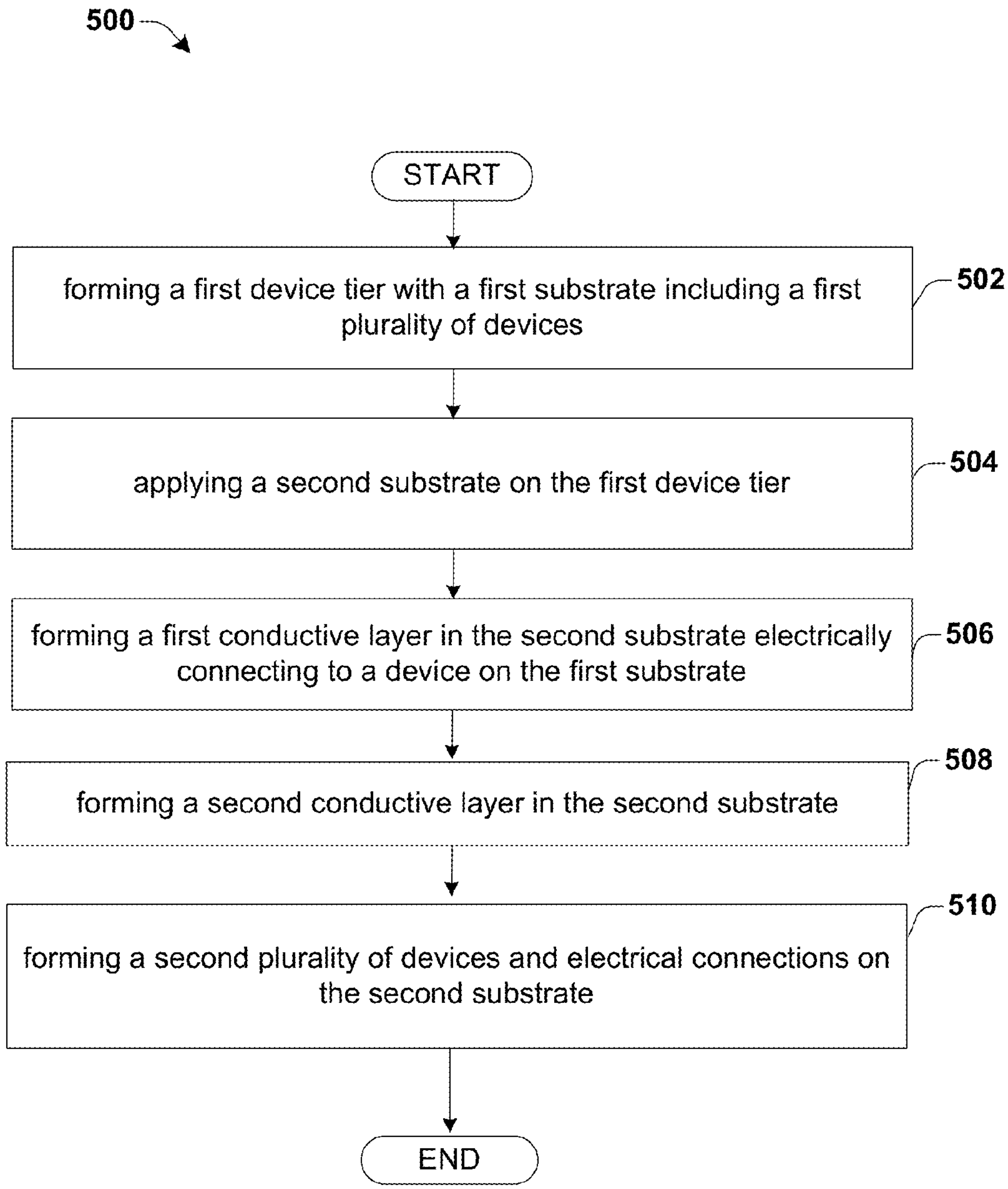


FIG. 4



500
START
forming a first device tier with a first substrate including a first plurality of devices
502
applying a second substrate on the first device tier
504
forming a first conductive layer in the second substrate electrically connecting to a device on the first substrate
506
forming a second conductive layer in the second substrate
508
forming a second plurality of devices and electrical connections on the second substrate
510
END

Fig. 5

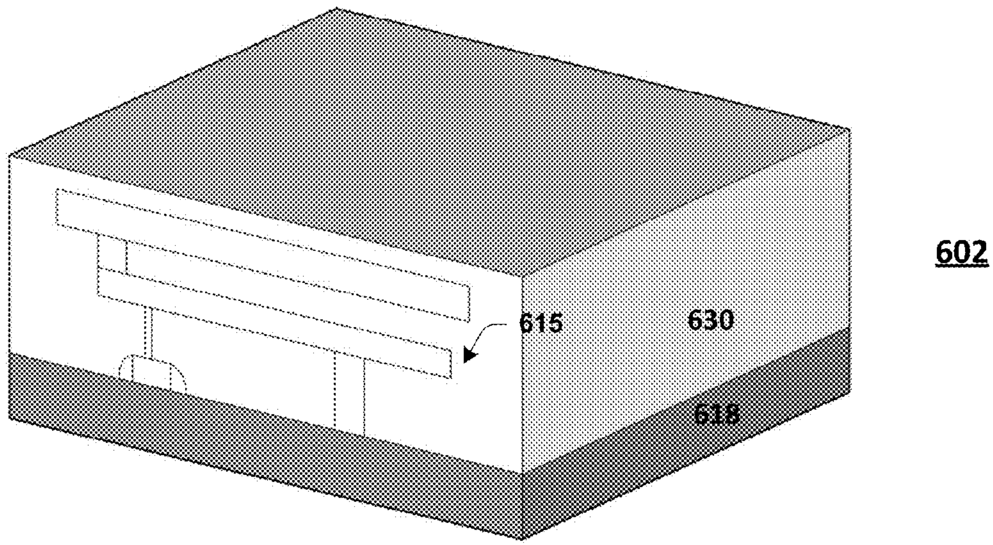


FIG. 6a

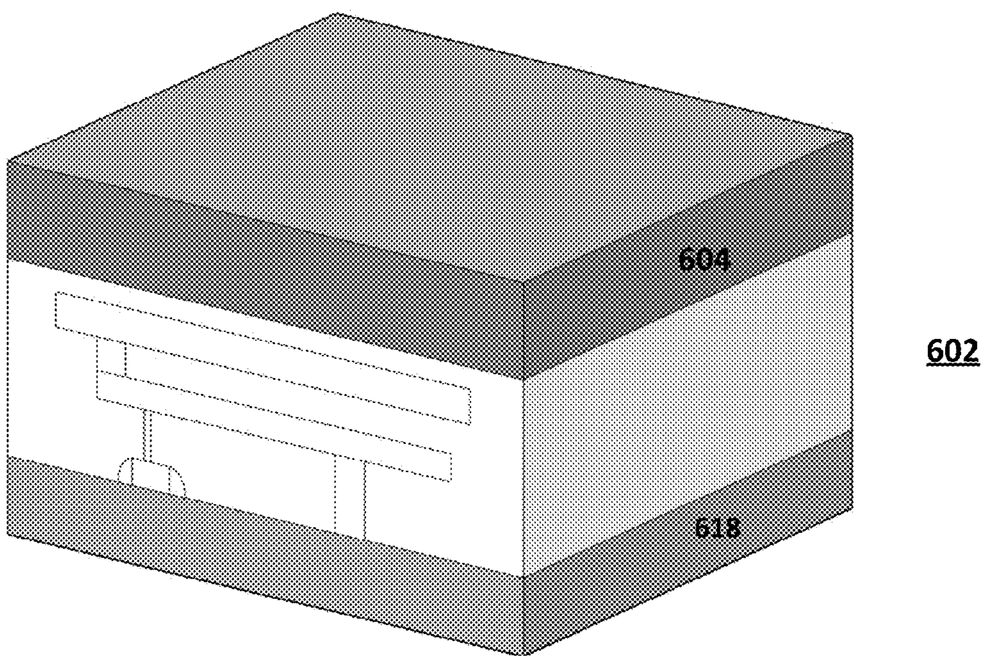


FIG. 6b

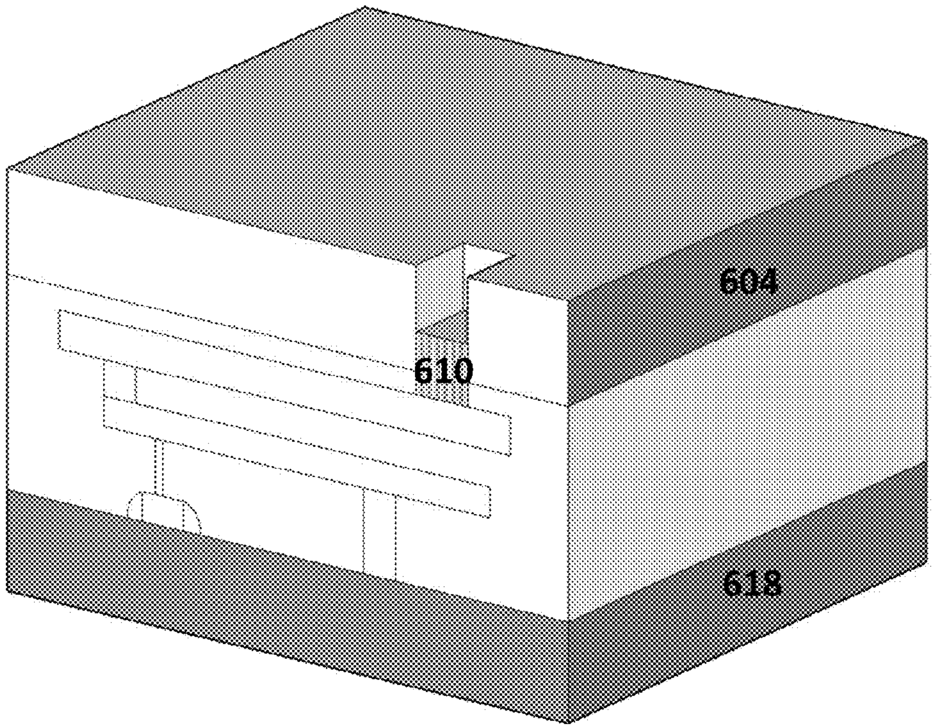


FIG. 6c

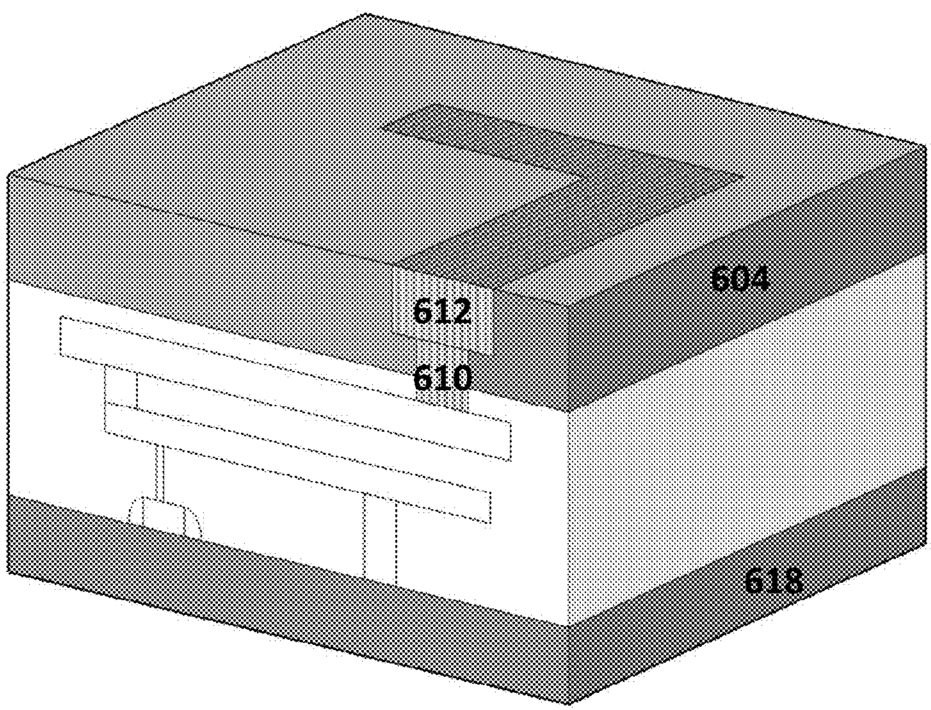


FIG. 6d

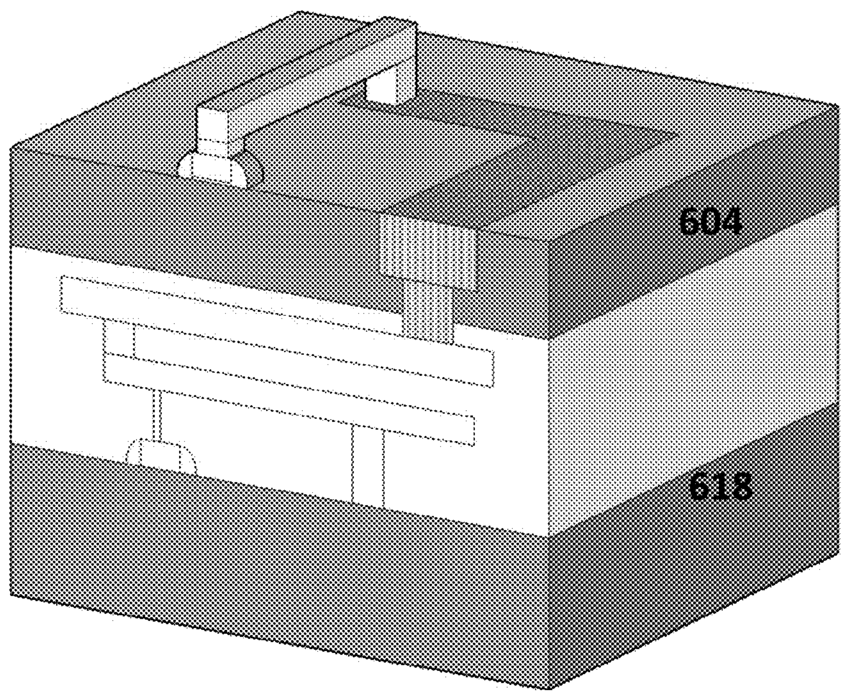


FIG. 6e

CONNECTING TECHNIQUES FOR STACKED CMOS DEVICES

BACKGROUND

A stacked CMOS chip is a kind of integrated circuit having multiple device tiers which are vertically stacked and which share one package. Stacked CMOS chips extend chip structure to three dimensions and increase the number of CMOS devices that can be "squeezed" into a given footprint.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates a perspective-sectional view of a stacked CMOS device in accordance with some embodiments.

FIG. **2** illustrates a perspective-sectional view of a stacked CMOS device in accordance with some alternative embodiments.

FIG. **3** and FIG. **4** illustrate perspective-sectional views of a three-step structure of a horizontal connecting structure and a four-step structure of a horizontal connecting structure.

FIG. **5** illustrates a flow diagram of some embodiments of methods for connecting stacked CMOS devices.

FIGS. **6***a*-**6***e* illustrate perspective-sectional views of some embodiments of methods for connecting stacked CMOS devices.

DETAILED DESCRIPTION

The description herein is made with reference to the drawings, wherein like reference numerals are generally utilized to refer to like elements throughout, and wherein the various structures are not necessarily drawn to scale. In the following description, for purposes of explanation, numerous specific details are set forth in order to facilitate understanding. It will be appreciated that the details of the figures are not intended to limit the disclosure, but rather are non-limiting embodiments. For example, it may be evident, however, to one of ordinary skill in the art, that one or more aspects described herein may be practiced with a lesser degree of these specific details. In other instances, known structures and devices are shown in block diagram form to facilitate understanding.

Relative to packaging solutions where multiple chips are arranged in separate horizontally spaced packages, stacked CMOS devices (which include multiple chips that are vertically "stacked" over one another in a single package), shrink the lateral footprint for the circuits when arranged within a product. However, the vertical dimension of stacked CMOS devices can become an issue in some applications. For example, stacked CMOS chips can be too thick for some ultra-thin apparatuses, such as cell phones or portable entertainment units. In addition, forming electrical connections between different vertical device tiers requires alignment of corresponding contact points on the corresponding device tiers, which limits flexibility in structure design. Therefore, in a stacked semiconductor integrated circuit in accordance with some embodiments, instead of connecting multiple tiers solely by a vertical interwafer via, a multi-layer horizontal connecting structure is fabricated inside a substrate of an individual device tier. Individual layers of the multi-layer horizontal connecting structure have different patterns as viewed from above the substrate. Relative to conventional approaches, stacked CMOS devices with multi-layer horizontal connecting structures provide several advantages. For example, locations of electrical contact points of different tiers are flexible, metal usage for electrical path layers is reduced, and the number of and/or thickness of electrical path layers is decreased which tends to "thin down" chip thickness. Power dissipation is also reduced.

FIG. **1** illustrates a perspective-sectional view of a stacked CMOS device **100** in accordance with some embodiments. The stacked CMOS device **100** includes multiple device tiers, such as a first device tier **102** and a second device tier **116**. The first device tier **102** comprises a first substrate **104** and a first plurality of devices **106**. The second device tier **116** comprises a second substrate **118** and a second plurality of devices **120**. A first inter-tier horizontal interconnecting structure **108** is formed at least partially inside the first substrate **104**. The first inter-tier horizontal structure **108** electrically connects one or more devices, such as device **106**, on the first substrate **104**, to one or more devices, such as device **120**, on the second substrate **118**. The first inter-tier horizontal interconnecting structure **108** can comprises multiple conductive layers, such as metal layers, with different patterns as viewed from above the first substrate.

The first inter-tier horizontal structure **108** includes a first conductive layer **110**, which takes the form of a vertical connection element in this example. The first conductive layer **110** is coupled to a second conductive layer **112**, which takes the form of a first horizontal layer in this example. The second conductive layer **112**, which takes the form of a first horizontal layer in this example, is disposed above the first vertical connection element **110** and is connected to a device of the first plurality of devices **106** or other contact paths on the first device tier **102**, for example, power, ground or signal pins. The second conductive layer **112** is electrically coupled to the device of the second device tier **116** by the first vertical connection element **110**. The first conductive layer **110** couples the second conductive layer **112** (and hence device **106**) to an electrical interconnect structure **115** on the second device tier **116**. The electrical interconnect structure **115** has multiple metal layers, such as **113** and **114**. These metal layers **113** and **114** are arranged under a back side of the first substrate **104** and are coupled to a device **120** of the second device tier **116**. The electrical interconnect structure **115** can also be coupled to other contact points of the second device tier **116** stacked under the first device tier **102**. The electrical interconnect structure **115** can either be formed in a dielectric layer between the first tier **102** and the second tier **116** or can be coupled into the second tier **116**.

The first plurality of devices **106** on the first substrate **104** and the second plurality of devices **120** on the second substrate **118** can be two dimensional structures (e.g., planar MOSFETs) or three dimensions structures (e.g., silicon on insulator (SOI) devices or FinFET devices). The first inter-tier horizontal interconnecting structure **108** in the first substrate **104** can be copper, silver, tungsten or aluminum with a Ta, Ti, TaN, TiW, TiWN or TiN barrier for preventing metal diffusions. A dielectric layer is formed surrounding the barrier layer for electrical isolation. The first substrate **104** can be either bulk Silicon or epitaxial Silicon on a dielectric material. To further reduce metal material, reduce layers, or decrease complexity of the electrical interconnect structure **115**, the first device tier **102** can have devices on both sides. The first device tier **102** can also be "flipped" over relative to what is shown in FIG. **1** so that a top side of the first substrate **104** with the first plurality of devices **106** is proximate to a top side of the second substrate **118** with the second plurality of devices **120**. In such way, electrical connections between the first plurality of devices **106** and the second plurality of devices **120** become more flexible. The first device tier **102** can be formed onto the second device tier **116** by deposition, spray coated, curtain coated, or spin coated. The first device tier **102** can also be bonded to the second device tier **116**.

Thus, FIG. **1** shows an example of a stacked CMOS device **100** with two device tiers (e.g., **102**, **116**) connected by a multi-layer inter-tier horizontal interconnecting structure **108** in accordance with some embodiments. Some advantages of this structure include improved placement and routing flexibility and reduced metal usage and further reduction of area and power consumption of the circuit.

FIG. **2** illustrates a perspective-sectional view of a stacked CMOS device **200** in accordance with some alternative embodiments. The stacked CMOS device **200** shows example embodiments of disclosure that a third device tier **226** with a third substrate **228** and a third plurality of devices (e.g., **232**) can be stacked onto a first device tier **202** and a second device tier **216** similar to **102** and **116** in FIG. **1**. More tiers can be stacked onto the third device tier **226**. A second horizontal connecting structure **230** inside the third substrate **218** comprises three layers **220**, **222** and **224** and electrically connects the first device tier **202** and the third device tier **226** of which a detailed example perspective-sectional view is shown in FIG. **3**. Notably, the first substrate **204** with the first horizontal connecting structure and the third substrate **228** with the second horizontal connecting structure can have similar or different structure. Horizontal connecting structures can have same or different numbers of conductive layers. Patterns of conductive layers can also be different. Thus, FIG. **2** shows another example semiconductor integrated circuit with more than two device tiers connected by multi-layer inter-tier horizontal interconnecting structures in accordance with some alternative embodiments.

FIG. **3** illustrates a perspective-sectional view of an example three-layer structure of a horizontal connecting structure. The horizontal connecting structure can be used as either the first horizontal connecting structure **208** or the second horizontal connecting structure **230** in FIG. **2**. In the example, a first conductive layer **320** is a first vertical connection element electrically coupled to a device of a device tier thereunder. A second conductive layer **322** is a first horizontal layer disposed above the first vertical connection element **320** and a third conductive layer **324** is a second horizontal layer disposed above the first horizontal layer **322** and electrically coupled to a device on a substrate **304** of a device tier **326** thereon through both the first conductive layer **320** and the second conductive layer **322**. A location of at least a portion of the first conductive layer **320** shifts horizontally to a location of the second conductive layer **322** or the third conductive layer **324**. The first conductive layer **320** connects contact points such as **326** and **328** on the other side of a substrate **304** not vertically aligned with a location of the first conductive layer **320** through the second conductive layer **322** and the third conductive layer **324**. The first conductive layer **320**, which is a vertical connection element in the illustrated example, can have a square-like or rounded perimeter as viewed from above and can fall within edges of second conductive layer. In some embodiments, **320** is formed along Z direction, **322** is formed along Y direction, **324** is formed along X direction. In some embodiments, **320**, **322**, **324** are in perpendicular with each other in respective X, Y, Z direction. In some embodiments, **304** includes any number of conductive layers. In some embodiments, any two conductive layers of the conductive layers in **304** are in parallel or in perpendicular with each other.

FIG. **4** illustrates a perspective-sectional view of a four-layer horizontal connecting structure **400** comprising an additional fourth conductive layer. The four layer horizontal connecting structure **400** can be used as either the first horizontal connecting structure **208** or the second horizontal connecting structure **230** in FIG. **2**. In FIG. **4**'s example, a first conductive layer **420** is a first vertical connection element extending in the z-direction and which is electrically coupled to a device of a device tier (not shown) thereunder. A second conductive layer **422** is a first horizontal layer disposed above the first vertical connection element **420** and extending in the y-direction. A third conductive layer **423** is a second vertical connection element connecting the second conductive layer **422** to a fourth conductive layer **424**. The fourth conductive layer **424** is a second horizontal layer which extends in the x direction and which is disposed above the second vertical connection element **423**. The first conductive layer **420** is electrically coupled to a device on a substrate **404** of device tier **426** through the second conductive layer **422**, the third conductive layer **423**, and the fourth conductive layer **424**. Structures of FIG. **3** and FIG. **4** can be applied to any upper level tier (e.g. the tier **102** of **100** and tier **202** or **226** of **200**) of disclosed stacked CMOS devices.

FIG. **5** illustrates a flow diagram of some embodiments of methods for connecting stacked CMOS tiers in accordance with some embodiments. While disclosed methods (e.g., methods **500** of FIG. **5**) are illustrated and described below as a series of acts or events, it will be appreciated that the illustrated ordering of such acts or events are not to be interpreted in a limiting sense. For example, some acts may occur in different orders and/or concurrently with other acts or events apart from those illustrated and/or described herein. In addition, not all illustrated acts may be required to implement one or more aspects or embodiments of the description herein. Further, one or more of the acts depicted herein may be carried out in one or more separate acts and/or phases.

At **502**, a first device tier with a first substrate including a first plurality of devices is formed.

At **504**, a second substrate is applied on the first device tier.

At **506**, a first conductive layer is formed in the second substrate electrically connecting to a device on the first substrate.

At **508**, a second conductive layer is formed in the second substrate.

At **510**, a second plurality of devices and electrical connections are formed on the second substrate.

One example of FIG. **5**'s method is now described with regards to a series of cross-sectional views as shown in FIGS. **6***a*-**6***e*. Although **6***a*-**6***e* are described in relation to method **500**, it will be appreciated that the structures disclosed in FIGS. **6***a*-**6***e* are not limited to such a method, but instead may stand alone as a structure.

At FIG. **6***a*, a first device tier **602** with a first substrate **618** and a first plurality of devices is formed. An electrical path **615** with multiple layers of metal is formed onto the first substrate inside a dielectric layer **630**. The multiple layers of metal can be copper, silver, tungsten or aluminum, for example.

At FIG. **6***b*, a second substrate **604** is applied on the first device tier **602**. The second substrate can be formed by deposition, such as epitaxial deposition for example, or can be bonded to the second device tier **116**. For example, in some embodiments, the first device tier can correspond to a first bulk silicon wafer, and the second device tier can correspond to a second bulk silicon wafer, wherein the first wafer has a backside (or topside) that is bonded to the topside of the second bulk silicon wafer.

At FIG. **6***c*, after the second substrate has been applied to the first substrate, a first conductive layer **610** is formed in the second substrate. The first conductive layer **610** electrically connecting to a device on the first substrate **618**. For example, the first conductive layer **610** can be copper, silver, tungsten or aluminum with a Ta, Ti, TaN, TiW, TiWN or TiN barrier (not shown) for preventing metal diffusions. A dielectric layer (not shown) is formed surrounding the barrier layer for electrical isolations.

At FIG. **6***d*, a second conductive layer **612** is formed in the second substrate **604**. For example, the second conductive layer **612** can be copper, silver, tungsten or aluminum with Ta, Ti, TaN, TiW, TiWN or TiN barrier for preventing metal diffusion, and also form dielectric layer surrounding the barrier layer for electrical isolation.

At FIG. **6***e*, a second plurality of devices and electrical connections are formed on the second substrate. One or more of the second plurality of devices on the second substrate are electrically coupled to one or more of the first plurality of devices on the first substrate.

Thus, some embodiments relate to a semiconductor integrated circuit (IC). The semiconductor integrated circuit comprises a first device tier with an first inter-tier horizontal interconnecting structure inside a first substrate and a second device tier being electrically connected to the first device tier by the first inter-tier horizontal interconnecting structure. The first inter-tier horizontal interconnecting structure comprises a first conductive layer and a second conductive layer with different patterns.

Other embodiments relate to an integrated circuit. The integrated circuit comprises a first substrate including a first plurality of devices and a first horizontal interconnecting structure disposed in the first substrate. The integrated circuit further comprises a second substrate including a second plurality of devices, the first and second substrates being electrically connected to one another so the second substrate is under the first substrate and the first horizontal interconnecting structure electrically couple one or more of the first plurality of devices to one or more of the second plurality of devices. The first horizontal interconnecting structure comprises a first conductive layer and a second conductive layer with different patterns as viewed from above the first substrate.

Still another embodiment relates to a method of fabricating stacked CMOS devices. In this method, a first device tier with a first substrate including a first plurality of devices is formed. A second substrate is applied on the first device tier. A first conductive layer is formed in the second substrate electrically connecting to a device on the first substrate. A second conductive layer is then filled in the second substrate. At last, a second plurality of devices and electrical connections are formed on the second substrate.

It will be appreciated that while reference is made throughout this document to exemplary structures in discussing aspects of methodologies described herein (e.g., the structure presented in FIGS. **6***a*-**6***e*, while discussing the methodology set forth in FIG. **5**), that those methodologies are not to be limited by the corresponding structures presented. Rather, the methodologies (and structures) are to be considered independent of one another and able to stand alone and be practiced without regard to any of the particular aspects depicted in the FIGS. Additionally, layers described herein, can be formed in any suitable manner, such as with spin on, sputtering, growth and/or deposition techniques, etc.

Also, equivalent alterations and/or modifications may occur to those skilled in the art based upon a reading and/or understanding of the specification and annexed drawings. The disclosure herein includes all such modifications and alterations and is generally not intended to be limited thereby. For example, although the figures provided herein, are illustrated and described to have a particular doping type, it will be appreciated that alternative doping types may be utilized as will be appreciated by one of ordinary skill in the art.

In addition, while a particular feature or aspect may have been disclosed with respect to only one of several implementations, such feature or aspect may be combined with one or more other features and/or aspects of other implementations as may be desired. Furthermore, to the extent that the terms "includes", "having", "has", "with", and/or variants thereof are used herein, such terms are intended to be inclusive in meaning—like "comprising." Also, "exemplary" is merely meant to mean an example, rather than the best. It is also to be appreciated that features, layers and/or elements depicted herein are illustrated with particular dimensions and/or orientations relative to one another for purposes of simplicity and ease of understanding, and that the actual dimensions and/or orientations may differ substantially from that illustrated herein.

What is claimed is:

1. A semiconductor integrated circuit (IC), comprising:
- a first device tier comprising a first dielectric layer disposed on a first semiconductor substrate, wherein a plurality of metal layers are disposed within the first dielectric layer and a first inter-tier horizontal interconnecting structure is disposed inside the first semiconductor substrate, and
- a second device tier being electrically connected to the first device tier by the first inter-tier horizontal interconnecting structure,
- wherein the first inter-tier horizontal interconnecting structure comprises a first conductive layer and a second conductive layer disposed on the first conductive layer with a different pattern than the first conductive layer.

2. The IC of claim **1**, wherein the first inter-tier horizontal interconnecting structure comprises:
- a first vertical connection element disposed in the first semiconductor substrate and electrically coupled to a device of the second device tier, and
- a first horizontal layer disposed in the first semiconductor substrate above the first vertical connection element and laterally extending to a position that is not vertically aligned with the first vertical connection element,
- wherein the first horizontal layer is electrically coupled to the device of the second device tier through the first vertical connection element.

3. The IC of claim **2**, wherein the second device tier further comprises
- an electrical interconnect structure arranged over the device of the second device tier, the electrical interconnect structure having an upper surface to which the first vertical connection element is coupled.

4. The IC of claim **1**, wherein the first inter-tier horizontal interconnecting structure comprises,
- a first vertical connection element disposed in the first semiconductor substrate and electrically coupled to a device of the second device tier,

a first horizontal layer disposed in the first semiconductor substrate above the first vertical connection element, and

a second horizontal layer disposed in the first semiconductor substrate above the first horizontal layer and being electrically coupled to the device through both the first vertical connection element and the first horizontal layer.

5. The IC of claim **4**, further comprising: a second vertical connection element disposed in the first semiconductor substrate and electrically coupling the first horizontal layer to the second horizontal layer.

6. The IC of claim **1**, wherein the first inter-tier horizontal interconnecting structure further comprises: a third conductive layer in the first semiconductor substrate and arranged in parallel or in perpendicular with the second conductive layer.

7. The IC of claim **1**, further comprising a third device tier being electrically connected to the first device tier by a second inter-tier horizontal interconnecting structure.

8. The IC of claim **1**, the first device tier has devices on both sides.

9. An integrated circuit, comprising:

a first device tier comprising a first plurality of devices disposed on a first semiconductor substrate;

a first horizontal interconnecting structure disposed in the first semiconductor substrate, wherein the first horizontal interconnecting structure comprises a first conductive layer connected to a second conductive layer, wherein the first conductive layer and the second conductive layer have different patterns as viewed from above the first semiconductor substrate;

a second device tier comprising a second plurality of devices disposed on a second semiconductor substrate, the second semiconductor substrate is under the first semiconductor substrate; and

wherein the first horizontal interconnecting structure electrically couples one or more of the first plurality of devices to one or more of the second plurality of devices.

10. The integrated circuit of claim **9**, wherein the first semiconductor substrate is deposited, spray coated, curtain coated, spin coated or bonded to the second semiconductor substrate.

11. The integrated circuit of claim **10**, further comprising:

a third device tier stacked onto the first device tier comprising a third plurality of devices disposed on a third semiconductor substrate; and

a second horizontal interconnecting structure inside the third semiconductor substrate.

12. The integrated circuit of claim **9**, further comprising a second semiconductor substrate including a second plurality of devices under the first semiconductor substrate wherein a first face of the first semiconductor substrate with devices thereon faces a second face of the second semiconductor substrate with devices thereon.

13. The integrated circuit of claim **9**, wherein the first horizontal interconnecting structure is copper, silver, tungsten or aluminum.

14. The integrated circuit of claim **9**, wherein the first horizontal interconnecting structure comprises a barrier layer made of Ta, Ti, TaN, TiW, TiWN or TiN, and a dielectric layer surrounding the barrier layer.

15. The integrated circuit of claim **11**, wherein the first horizontal interconnecting structure and the second horizontal interconnecting structure have same or different numbers or patterns of conductive layers.

16. A stacked CMOS device, comprising:

a first device tier comprising a first device disposed over a first semiconductor substrate;

a second device tier stacked over the first device tier and comprising a second device disposed over a second semiconductor substrate; and

an interconnecting structure configured to electrically connect the first device tier and the second device tier, which is disposed within the second semiconductor substrate and that comprises a first connection point at a lower surface of the interconnecting structure facing the first device and a second connection point at an upper surface of the interconnecting structure facing the second device, wherein the first connection point and the second connection point are not vertically aligned;

wherein the interconnecting structure comprises a first conductive layer extending horizontally to connect the first and second connection points.

17. The stacked CMOS device of claim **16**, further comprising:

a vertical connection element extending into the second semiconductor substrate and physically connecting the first connection point to an underlying metal layer disposed within a dielectric layer.

18. The stacked CMOS device of claim **16**, wherein the interconnecting structure further comprises:

a second conductive layer disposed above the first conductive layer and having a different pattern from the first conductive layer;

wherein an upper surface of the second conductive layer is co-planed with an upper surface of the second semiconductor substrate.

19. The stacked CMOS device of claim **16**, wherein the interconnecting structure further comprises:

a second conductive layer arranged in parallel or in perpendicular with the first conductive layer as viewed from above the second semiconductor substrate and connected to the first conductive layer through a vertical connection element disposed therebetween.

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